

# Standardizing Video-Based Avionics and Mission Systems around the ARINC 818-3 Video Bus

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**Abstract**— Modern aircraft rely more and more on a variety of optical and infrared of sensors that are used for avionics (navigation, landing assistance (EVS)) and missions (target tracking, aircraft protection (counter measures), and ISR). Video-based avionics and mission systems employ different video protocols and buses: including both digital-SDI, SMPTE 292, HDMI, Display Port, Ethernet (AFDX, TSN, TTE), ARINC 818 and analog (RGB, RS-170, CVBS). The latest generation of cockpit and mission displays (HUDs, HDDs, HMDs) all utilize ARINC 818-3 as the video protocol of choice due to some specific technical features that are only present in ARINC 818-3. With such a variety of options of video buses and protocols available, how would a system designer decide which protocol(s) to use and how to best integrate them into a low-latency, high-resolution system? Adding to the challenge, the cost of development and certification of equipment is prohibitive in many cases. System designers don't have a clean sheet of paper, but must integrate older, but certified equipment with newer, higher performance hardware. Performance and cost trade-offs are always present, and even many of the newest systems require combining old and new technology to meet the design and cost goals. This work is a follow-on from the paper *Interfacing and Testing High-Resolution, Video-Based Avionics and Mission Systems that Use ARINC 818-3* presented at DASC 2023.

This paper will discuss the challenge of integrating a variety of video protocols, discuss key features and benefits of each protocol, and explore why ARINC 818-3 is becoming the de-facto standard not only as a display interface, but as a system level bus being used from sensors, to processors, to displays. No other currently available protocol can meet all the technical requirements to serve as the primary video backbone for avionics and mission systems in commercial and military aircraft.

The key technical features of different protocols including: SDI, HDMI, Display Port, Ethernet (AFDX, TSN, TTE), and ARINC 818 will be examined. Complex avionics and mission systems architectures need to accommodate multiple different protocols, including both digital and analog. The strengths and weaknesses of each protocol is discussed to help designers understand system level tradeoffs

We examine key system level-design parameters of the different digital video protocols, including:

**Minimizing sensor to display (or decision) latency, timing precision required for digital displays, flexibility (bandwidths), accommodating both video and data, conversion to/from other protocol standards and pixel types, video concentration (multiple video streams on a single link).**

Finally, the paper shows why ARINC 818-3 is the best option as the video backbone, and how it can be integrated and interfaced with all the other video protocols and buses. In addition, it points out key design considerations that must be planned at a system level when integrating infrared and optical sensors, video and mission processors, and multiple display types (HDDs, HMDs, HUDs).

**Keywords**— *Video Protocols, Video Bus, ARINC 818, Ethernet, AFDX, TTE, TSN, Mission Systems, Avionics, Infrared, Sensors, ISR, Displays, UAP, IMA, Autonomous*

## I. INTRODUCTION

Modern commercial and military aircraft use a variety of different buses for moving mission-critical video and data throughout the aircraft, from sensors, video and mission processors, and displays (HUDs, HDDs, HMDs). Avionics and mission system architects have a difficult job of trying to balance the need for multiple buses. Ideally, one “bus” would be capable of all the video and data needs of an aircraft. As the next generation of aircraft are being designed, the desire to simplify is ever present. The Airline Engineering Electronics Subcommittee has formed the Next Generation Network Technology for Avionics Communication subcommittee to explore the next generation of databuses, looking to replace lower speed, but simple technologies such as ARINC 429, CAN, and Mil-STD 1553, with a higher-speed, mission-critical bus. This subcommittee is looking at different Ethernet-based technologies such as Time Sensitive Networking (TSN), Time-Triggered Ethernet (TTE), and an updated version of AFDX (ARINC 664p7).

This paper explores the unique challenges of high-speed, mission-critical video and how it differs from networked data, and consequently the different buses required to distribute data and video throughout the aircraft. Especially as deterministic Ethernet protocols proliferate, these protocols will be compared and contrasted with video specific protocols to understand their suitability as a mission-critical video bus.

We begin by clarifying the type of video focused on: uncompressed, high-resolution, high-speed video used by optical and infrared sensors, video and mission processing systems, and a variety of cockpit displays. Uncompressed video is used because of the fidelity needed, the low latency requirements, and the certification and safety concerns. Compression techniques are usually lossy (meaning key information may be lost required for the highest fidelity applications) and add latency for compression and decompression.

Fig. 1 shows a representative avionics and mission system video architecture in an attack helicopter, but many elements are also representative of systems used in commercial applications.

Starting at the bottom of the image, electro-optical and infrared sensors are packaged in a pod, the video from that pod is fed over a concentrated link to a video switch. Other optical sensors are also fed into the switch. In some instances, a pilot may want to see the raw sensor video, and at other times, the fully processed video. The video switch is integral to the architecture, connecting sensors, video processors, Head Down Displays (HDD), Large Area Displays (LAD), and either Head Up Displays (HUD) or Helmet Mounted Displays (HMD).

Many elements of this reference architecture also apply to large commercial aircraft. Instead of each pilot having a single LAD, there are up to five large displays, plus two HUDs. They may not have a sensor pod for targeting, but instead a Synthetic or Enhanced Vision System (S/EVS) like a Collins EVS 3600 which has infrared and optical sensors built in.

The video is typically processed in real-time and could require sensor fusion techniques, symbology overlays, and object tracking. The nature of these systems requires very low latency from sensor, to processor, to display. In some cases, such as target tracking, the video is not used to display in the cockpit, but to send precise coordinates to other avionics or mission systems. For example, destroying or disabling an incoming missile using a laser, missile, or

directed energy weapon. The end-to-end latency requirements for such systems is typically in the milliseconds to tens of milliseconds range. This architecture is only showing the video connection, and in addition, almost every device will have a data bus connection for command and control, which could be ARINC 429, Mil-STD 1553, AFDX, or other data buses. In some cases, the video bus can be used for command and control of the device since they all have provisions for ancillary or meta data that can be sent along with the video.

Before examining video bus characteristics, it is essential to understand two key factors that influence video bus architecture and the choice of which video bus(es) will be used: end-to-end latency and the precise timing required by mission-critical cockpit displays.

## II. LATENCY

System latency is important both for military and commercial applications. HUDs or HMDs with S/EVS are common on larger commercial aircraft, and are used to improve the landing floor during low visibility due to weather or darkness.

According to research done by NASA related to the impact of latency on pilots using HMDs or HUDs together with an S/EVS, they recommend the following.

“Based upon the most stringent requirements for HMD applications of S/EVS (i.e., demanding tasks using a high resolution, large field-of-view head-worn display), the system latency must be less than 20 msec.”[3].

“From SAE ARP 5288, HUD boresight requirements are stipulated to minimized display errors to be consistent with the intended function of the HUD. The allowable display error for a conformlal HUD as measured from the HUD eye reference point is less than 5 mrad (0.286 deg). With this requirement, system latency less than 25 msec would be required for very slow head-rates (i.e., 10 deg/sec head-rate equates to 0.286 deg/10 deg/sec ~ 25 msec latency). Head movements of more than 100 deg/sec would require less than 2.5 msec system latency to remain within the allowable HUD error levels. Head rates of 100 deg/sec should, by no means, be considered excessive in commercial transport operations.”[3].

“HMD system architectures can be designed for minimum latency, which will approach this latency requirement, but to meet this requirement will likely require video update rates greater than the present standard of 60 Hz.”[3].

This research indicates that for HMDs and HUDs, the sensor to pilot latency must be minimized, and with targets in the 20ms range and below in some circumstances. Although other research has suggested that HMD latency of 50ms is acceptable, the authors of the NASA study believe that is only the case in lower pilot demand situations. There are cases where the latency should be kept to 2.5ms. System architects need to understand the use cases including details

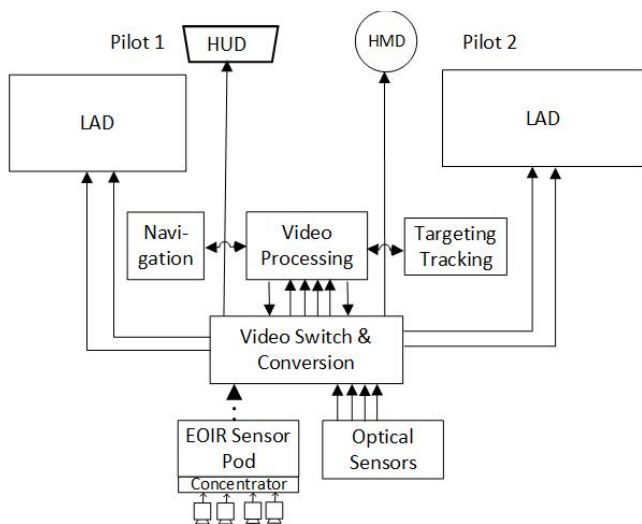


Fig. 1. Overview of real-time, mission-critical video system

of the technology as well as pilot workloads when establishing latency requirements.

When image processing is done, such as sensor fusion used for S/EVS systems it typically requires image buffering. This alone could take the majority of the latency budget, if not exceed the 20ms target. This would leave little latency budget for converting from one video format to another, for example, HD-SDI to ARINC 818 which usually requires frame buffering. This paper focuses on the impact of the video bus and architecture on latency, but not the processing required, which is independent of the video bus choice and rather depends on the algorithms used and the platform executing the algorithms.

A simplified diagram of a video-based architecture for avionics and mission systems is shown in Fig. 2 for a discussion on end-to-end latency considerations.

Eight sources of latency can be identified in Fig. 2: sensor to EVS processor, EVS processor, sensor or EVS to video switch, video switch and converter, video switch to display processor, display processor, processor to display, and finally, the display.

#### A. Sensors to S.EVS Processor

Moving video from the sensor to the S/EVS processor can be done very efficiently, or may add a video frame or more of delay. One solution is to have the video processing (such as sensor fusion) packaged together with the sensors themselves (shown in the dashed line), as commercially available S/EVSs do. The sensors need to be triggered (synchronized) together. In cases where the sensors are not located with the video processor, video concentration (putting all the video signals on a single link) may be beneficial to the system architecture. Our previous paper showed that low latency video concentration architectures when done properly, the range of latency is 75 $\mu$ s for frame synchronous designs and a video frame for line synchronous [1].

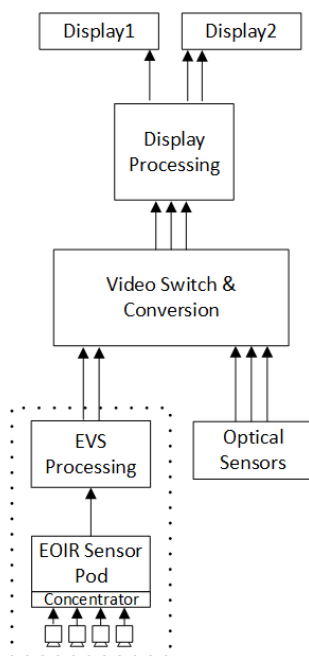


Fig. 2. Simplified signal flow for latency consideration

#### B. S/EVS Processor

These require sensor fusion, which may include registration (aligning pixels), overlaying the IR/Optical pixels, and weighting them. Typically, this process will require partial or full frame buffering in addition to the processing itself. The sensor inputs should be closely synchronized, and ideally, at the same update rate (for example, 100Hz) and same video resolution (for example, 1280x1024). If video scaling is required (for example, 1280x1024 to 1920x1080: this requires changing both resolution and aspect ratio) and/or frame rate conversion (for example, 50Hz to 100Hz), these can add up to a frame of latency. This is the first major source of latency and will be in the tens of milliseconds range, depending on the algorithms used and processing power available.

#### C. Sensor and EVS to Switch

Ideally, the EVS would output video using frame or line synchronous timing, and both the EVS output and any other sensors would use the same video protocol and video link rate (for example, 4.25Gbps). Video lines can be output as soon as they are available. Packing the video lines and sending them can be slaved to the timing of the output of the EVS or sensor. The latency of this stage should be in the tens of microsecond range.

#### D. Switch and Converter to Display Processor

If the incoming video is all using the same link rate, update rate, and the same protocol, then the latency of this stage can be in the tens of microsecond range. If video conversions are required (for example HDMI 60Hz to ARINC 818 100Hz), this will add up to one video frame of delay. Minimizing the number of video bus conversions is important to reduce latency, but often financial impacts are a large driver in selecting sensors.

#### E. Video Switch to Display Processor

Once the video signals are all converted to the same protocol and link rate, the video switch is outputting line synchronous or frame synchronous timing. The latency of this stage should be in the tens of microsecond range.

#### F. Display Processor

At this stage, video will be processed and superimposed with symbology, and pre-warped if required. This stage is a large source of latency, and can be in the millisecond to tens of milliseconds range. There are financial, certification, and safety trade-offs in determining if the display processor should be located in the display.

#### G. Display Processor to Display

Many displays include processing directly in the display (often called “smart displays”), the advantage is that no additional transition of video is required, the disadvantage is in certifying a display with the additional display processing built in is much more difficult due to the magnitude of software involved. When the display processor is not located in the display, then the packetizing of the video and sending

it with line synchronous timing may add additional latency. This could be in the tens of microseconds to tens of milliseconds range. If the display requires strict line synchronous timing, then buffering is usually required.

#### H. Display

If the display inputs line synchronous timed video, has no image buffer, and uses only FIFOs, then the latency at this stage is in the tens of microsecond range. If the display has memory buffers, then it will be in the tens of milliseconds range.

#### I. Latency Consideration Overview

Given all the possible sources of latency, careful consideration of the architecture is important, especially considering where image buffers are required. A poorly designed system may require buffering at three to four stages, which could introduce 50ms or 100ms in additional latency, without accounting for the S/EVS or display processing required. In contrast, careful consideration of the architecture and sources of latency (eliminating frame rate conversion, video format conversion, and locating processing inside S/EVS or displays) could yield an architecture requiring only one or two video frames of delay (not including processing time). As mentioned in the NASA study, using higher frame rates on sensors or displays may be a way of reducing latency. For example, buffering a video frame at 60Hz means a 16.66ms delay, whereas buffering a frame rate of 180Hz introduces a third as much latency. However, higher frame rates also typically mean higher costs. Picking a sweet spot for sensor frame rates to balance required performance, latency minimization, and required processor speeds is one of the challenges system architects always face.

Now that the importance of latency considerations has been discussed, the particular video timing requirements of mission system displays is developed by discussing timing synchronization classes, timing precision, and video centric special characters.

### III. SYNCHRONIZATION CLASSES AND COCKPIT DISPLAYS

Uncompressed video can be categorized into four different timing classes: asynchronous, frame synchronous, line synchronous, and pixel synchronous. There are a variety of Ethernet data buses that can move asynchronous video because it imposes no specific timing on the link. In many noncritical systems, asynchronous video is sufficient. As we move to flight and mission-critical systems, video latency and jitter becomes a major factor and synchronous video is required (frame, line, or pixel).

Of the three timing classes used in new aerospace mission-critical systems, frame and line synchronous are the most common.

#### A. Frame Synchronous

Frame synchronous is the least restrictive type of synchronous video, it imposes timing constraints on the

delivery of a whole video image, for example 60Hz. As long as the full image is delivered in that time (16.66ms for a 60Hz update rate) then the frame synchronous timing is met. The tolerance (jitter) of a video frame may be in the hundreds of microseconds range to milliseconds.

#### B. Line Synchronous

Line synchronous timing requires tight timing control on each video line, for example, 15.463 micro seconds per video line for a 1920x1080, 24-bit color at 60Hz video stream. The tolerance (jitter) on the delivery of these video line is often required to be 5 to 10 nanoseconds, but could be below two nanoseconds in some implementations.

#### C. Pixel Synchronous

Pixel synchronous is the most stringent timing class, and is typically achieved by embedding a clock signal along with the pixel data. An example of this is HDMI, which includes four pairs of signals, one for clock, and then one for each color of a pixel: R, G, and B. Pixel synchronous interfaces like HDMI are used in many desktop monitors and in some aircraft displays, but are very limited in distance and restrictive in other features.

### IV. TIMING PRECISION REQUIRED BY COCKPIT DISPLAYS

Modern cockpit displays often do not use any image buffers for safety and certification reasons, or due to latency issues. Displays must be certified to DO-254 to Design Assurance Level (DAL) A or B. These DALs indicate that if the system fails, loss of life or serious injury is possible or likely.

Part of the certification is proving that no erroneous or misleading data is possible or present. If the display contains image buffers, they can be a source of stale data, that is, pulling the same (stale) image from a memory buffer over and over and displaying it. Stale images would contain misleading or erroneous data. One way to avoid this source of misleading data is to build displays that do not include full image buffers, but rather only line FIFOs that store a few video lines worth of pixels. The fact that there are no memory buffers in a display and they only have FIFOs is what imposes the strict line synchronous timing on video transmitters. If the timing is slightly off, it is easy to over or under run a FIFO, causing the display to blank out. As an example, the way that timing is adjusted on a video line (as shown in Fig. 3) is by inserting "idle" characters. In ARINC 818 (below 10.0Gbps) and IDLE Order Set is 32 bits long. In the case of a 1080p resolution over a 4.25Gbps link, this correlates to 9.41 nanoseconds per IDLE Ordered Set. On a project GRT worked on in recent history for a modern commercial aircraft, the display was so sensitive to the timing that the idle characters between video lines had to be "dithered". Using 8 idle characters between video lines overran the FIFO, and 7 characters underran the FIFO, causing the display to blank out. This implementation required the transmitter to alternate between 7 and 8 idles between video lines, representing no more than 5ns of timing variation (jitter).

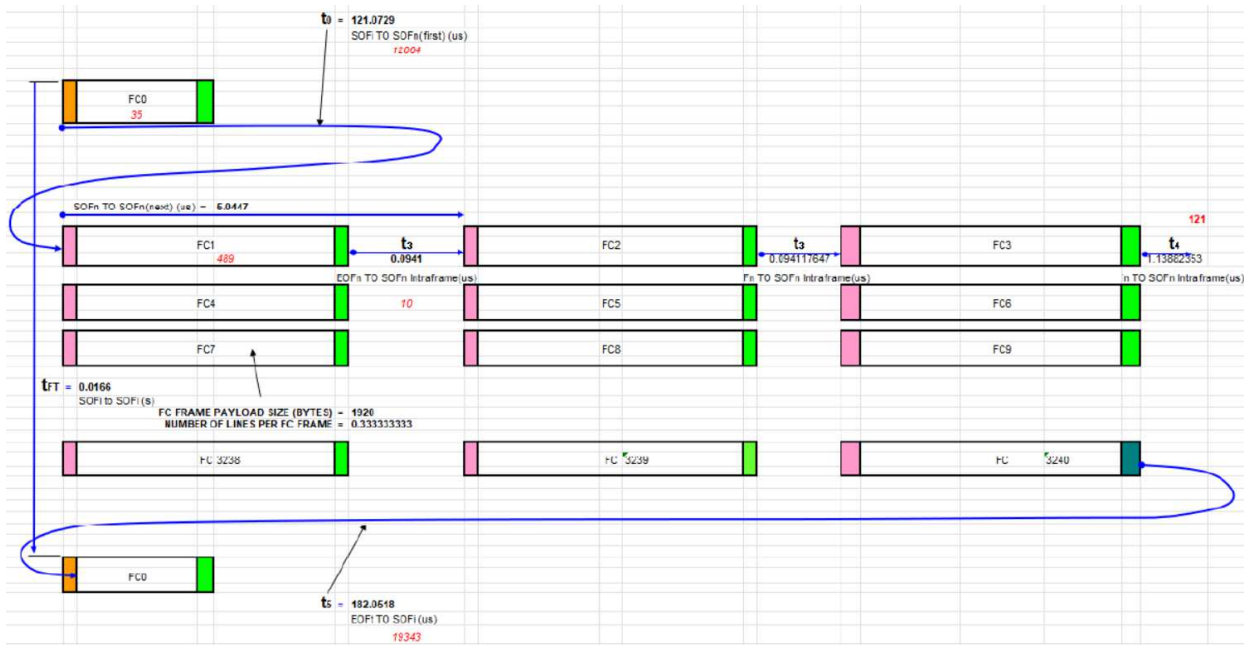


Fig. 3. Video timing for a HD image transmitted using ARINC 818 with line synchronous timing

Achieving line synchronous video timing also includes parameters required to precisely set vertical blanking,  $t_0$  and  $t_5$  shown on Fig. 3. Setting line timing is accomplished by setting  $t_3$  and  $t_4$ . These values must be precise,  $t_3$  in this example is 10 IDLE characters and  $t_4$  is 121 IDLE characters.

### V. VIDEO CENTRIC SPECIAL CHARACTERS

Precise control of video timing is also accomplished by having video centric special characters. Special characters means that they are distinguishable from data because of the bits set in the 8B/10B encoding. Video protocols (HDMI, SDI, ARINC 818, DisplayPort) have ways to distinguish video lines and video frames, and to set the “blanking” periods-the time during the transmission of a video image that does not contain pixel information. All video-centric protocols will have similar mechanisms.

Now that the type of video system is established and the exacting nature of video display timing and extremely tight latency requirements have been described, the characteristic of the video interfaces and options for video buses is explored.

### VI. COMPARISON OF VIDEO BUSES

Table 1 shows the comparison of four different video interfaces: HDMI, SDI (representing the family of SDI and SMPTE interfaces), ARINC 818, and DisplayPort. Other buses such as GigE Vision, CoaxPress which are used extensively in industrial applications are not discussed.

Since ARINC 818 was the only video protocol designed specifically for mission-critical cockpit applications, it has the widest feature set for avionics and mission systems. The

key distinguishing features of ARINC 818 that make it the best choice for mission-critical video systems include:

- Four timing classes provide options for moving any time class of video including precise timing required for cockpit display interfaces.
- Ability to be adapted to any pixel type.
- Highest number supported link rates means that designers do not have to overdesign a system. FPGA costs increase with the supported link rate, offering a variety of rates means that a designer can often choose a lower cost FPGA.
- Ability to do video concentration is helpful in systems with remotely located sensors so only a single fiber is required to move video from multiple sensors.
- Built in source and destination IDs in each packet. As a packetized protocol, utilizing source and destination IDs is essential both for video switching and for video concentration/deconcentration/filtering.
- Ability to work with Regions of Interest (ROI). A region of interest can be defined (for example for tracking a missile), and the rate of the ROI could be increased. For example, the complete image can be on a link (ie 100Hz), but once a region of interest has been defined, the rate of transmission for that ROI can be increased for high-speed tracking (i.e. 1000Hz or even 10,000Hz). Multiple ROIs can be defined.
- Optional full video image Cyclic Redundancy Checks (CRC), this adds an additional layer of confidence and system integrity, utilizing both packet and image CRCs.

TABLE I. COMPARISON OF VIDEO BUS FEATURES

	Video Buses			
	<i>HDMI</i>	<i>SDI</i>	<i>ARINC 818</i>	<i>DisplayPort</i>
Main Uses	Computer Monitors	Cameras, broadcast equipment, sensors	Certifiable Cockpit displays, sensors, video processors	Computer Monitors
Rates (Gbps)	4.95, 10.2, 18.0, 48	1.485, 2.97, 5.94, 12	1.0625, 2.125, 3.1875, 4.25, 5.0, 6.375, 8.5, 10.0, 12.0, 14.025, 21.0375, 28.05	10.8, 21.6, 32.4, 80.0
Metadata	Yes	Yes	Yes	Yes
Async	No	No	Yes	Yes?
Frame Sync	No	Yes	Yes	Yes?
Line Sync	No	Yes	Yes	Yes?
Pixel Sync	Yes	Yes	Yes	Yes?
Video Concentration	No	Yes	Yes	Up to 63 streams
Switching (Source ID/ Destination ID)	No	No	Yes	Yes
Data Only Mode	*No	*No	Yes	*No
Regions of Interest	No	No	Yes	No
Camera Synchronization	No	No	Yes, sync on SOFi	No
Packetization	No	Yes	Yes	Yes
Line CRC	No	Yes	Yes	Yes
Image CRC	No	No	Yes	No
Mixed Rate Transmission	No	No	Yes	No
Pixel Types	RGB, YCbCr	YCbCr, RGB	RGB, YCbCr, Mono BAYER, ARGB	YCbCr, RGB
Typical Physical Layer	Copper, up to 5m	Coax, up to 100m	Fiber, 100+ m	Copper, 15m
Signal Type	4 parallel	Serial	Serial	4 Parallel
Strengths	Low cost	Low cost, good distance over coax, flexibility	Extreme flexibility, features for avionics and mission systems, Simpler	Highest video resolutions, very flexible

- Defines how to use the protocol to trigger (synchronize) cameras.
- Allows mixing more than one update rate on the same link. For example, one link can carry an image at 60 Hz, and another at 180 Hz (such has symbology).
- Dozens of DAL A projects already certified.

VII. ETHERNET FOR LOW-LATENCY, UNCOMPRESSED AEROSPACE VIDEO

Ethernet protocols are the backbone of high-speed aircraft data buses and are indispensable for data networks. They have features optimized for data transmission, such as full-duplex operation, determinism, and switched topologies to be able to accommodate many nodes. In this paper, the focus is on video rather than data for mission-critical aerospace applications. Given the success of Ethernet protocols for data applications in aerospace, the question is

posed, is it possible to use Ethernet as the exclusive mission-critical video bus as well?

Four Ethernet protocols will be discussed Best Effort Ethernet (IEEE 802.3), ARINC 664p7 (AFDX®), TTE (Time-Triggered Ethernet AS6802), and TSN (Time-Sensitive Networking IEEE 802.1).

The most common in aviation is AFDX. Conversely, TTE has seen widespread adoption for spacecraft applications, being selected as the data network backbone for the NASA Artemis program and the EASA Ariane 6 launcher. TTE is also poised to be deployed in a variety of commercial and military aircraft, including as the data network for the Honeywell Anthem cockpit and as the flight controls network for the Boeing RASCAL program. Finally, in addition to a lengthy pedigree in the automotive and industrial automation industries, TSN has been baselined as the digital backbone technology for the upcoming Bell V-280 Valor Future Long Range Assault Aircraft.

A short description of each technology is provided below, paired with Table 2 which includes a review of features as well as the strengths and weaknesses of each data technology. Finally, this paper evaluates Ethernet for suitability to mission-critical video-based avionics and mission systems.

### A. Best-Effort Ethernet

Best-Effort Ethernet (BEE), defined in the IEEE 802.3 standard, is Commercial-Off-the-Shelf (COTS) Ethernet technology and is present in low-design assurance equipment ruggedized for military suitability. BEE is so called because data packets on a Best-Effort network may be lost or delivered out of order with no inherent method to inform the sending node of such. BEE is therefore not deterministic for anything but the most trivial of network topologies. However, Best-Effort networks can provide a high level of bandwidth for applications that require large amounts of data to be transmitted quickly. Additionally, Best-Effort is typically less expensive to implement and update than deterministic Ethernet networks, although introducing additional traffic without rate-constraints can substantially and adversely impact the system behavior. Overall, BEE offers a high-degree of maturity and flexibility but falls short

when assessed for robustness and certifiability.[1]

### B. Time-Triggered Ethernet AS6802

TTE uses a time-synchronized Ethernet network to deliver Ethernet frames on a set schedule, ensuring the reliable and timely transmission of data. TTE uses the concept of virtual links, where each desired unidirectional connection between two network end systems is established in the network configuration with a set of constraints that describe the requirements on the data to be transmitted. In a TTE network, a statically configured schedule combined with a shared notion of time between all nodes on the network allows for the deterministic delivery of Ethernet data with a known low latency and with jitter reduced to the order of microseconds. In an avionics context, this can be a major advantage because it allows for the transmission of critical data such as aircraft control information with low latency and a high degree of reliability and predictability. TTE was originally developed for safety-critical, highly-reliable aerospace systems with certifiability as a priority.

It should be noted that all products currently on the market that support Time-Triggered Ethernet also support transmission of AFDX and BEE traffic in addition to TTE. All three can be transmitted and received simultaneously

TABLE II. COMPARISON OF ETHERNET PROTOCOLS FOR AEROSPACE DATA NETWORKS

	Ethernet Protocols			
	<i>Best Effort</i>	<i>TTE</i>	<i>AFDX</i>	<i>TSN</i>
Optimized Applications	Lower-Criticality, High-Bandwidth, frequently upgraded applications	Safety & Mission Critical applications (e.g., flight-control, power-control, engine-control)	Safety-Critical applications (e.g., power-control and engine-control)	Mission-Critical applications
Rates Supported	Up to 100Gbit/s or beyond	Up to 1Gbit/s	Up to 100Mbit/s	Up to 40Gbit/s
Robustness	Limited	Full – when configured	Full – when configured	Moderate
Aerospace Certifiability	No DAL certification	DAL A	DAL A	No DAL certification currently – best suited for low DAL
Determinism	No	Full	Full	Deterministic only with proper network configuration
Traffic Scheduling	None	Fully scheduled offline network configuration	Fully scheduled offline network configuration	Dynamic stream configuration possible  Fully scheduled offline network configuration more typical in aerospace
Clock Synchronization	None	Distributed fault-tolerant clock synchronization	None	Non-fault tolerant GrandMaster (GM) clock sync via 802.1AS-2020
Maturity	High – TRL 9	High – TRL 9	High – TRL 9	Med – TRL 5/6 for aerospace
Strengths	Ultra-High bandwidth Low cost Easily upgraded	High-Bandwidth Ultra-low latency (~10 μs) Ultra-low jitter (~1 μs) Deterministic	Low Latency (~10 ms) Low Jitter (~1 ms) Deterministic	Flexible Higher-Bandwidth
Weakness	No determinism Not certifiable	Rigid network schedule	Bandwidth allocation wastes network capacity in exchange for determinism	Unproven certifiability Integration complexity GM clock single point of failure for synchronous applications

over a single unified physical infrastructure, reducing size, weight, and power requirements.

### C. AFDX

ARINC 664 part 7 (also known as AFDX®) is a rate-constrained deterministic Ethernet protocol. In a similar fashion to TTE, AFDX uses virtual links in place of traditional MAC addresses to route data through the network. However, rather than transmitting Ethernet frames on a set schedule between synchronized nodes as is the case with TTE, AFDX instead constrains the amount of bandwidth allocated to each virtual link. By allocating a total bandwidth for all virtual links that sums to less than the total bandwidth of the network, determinism is achieved, but it is inefficient.

### D. Time-Sensitive Networking

TSN refers to equipment adhering to the set of Ethernet extensions under development by the IEEE 802.1 TSN Working Group. TSN is an evolution of the IEEE Audio Video Bridging (AVB) networking standard originally designed for audio/video streaming and has evolved into use in automotive and industrial real-time control applications. A base set of extensions supporting asynchronous communication including a Credit Based Shaper, Frame Replication and Elimination, and Per-Stream Filtering and Policing is typically expected to be supported by most TSN devices. In addition to these features, synchronous communication requires additional extensions in the form of 802.1AS-2020 Time Synchronization and a Time Aware Shaper. TSN offers flexibility in its implementation of fault-tolerance and redundancy by shifting some of those considerations to the software application level to be implemented if desired. It also offers flexibility in achieving deterministic Ethernet communication via either synchronous or asynchronous means at the cost of greater integration complexity through its wide array of extensions.

### E. Ethernet Protocol Overview

It should be noted that all the above four technologies are open Ethernet standards, allowing the system architect to deploy them as needed and in combination with each other based on the specific use case and program requirements.

Each Ethernet bus is optimized for different data-centric applications, we now turn to exploring the suitability for mission-critical, low latency, uncompressed video for interfacing with sensors, processors and displays. Key to this

discussion is the nature of the video application. All the Ethernet protocols can carry compressed video streams that are not time critical, for example, moving video to a flight video recorder.

As an example, three video resolutions are explored in Table 3. These represent: HD (1920x1080) at 60Hz, 4K (3840x2160) at 30Hz and 60Hz, and 8K (7680x4320) at 25 Hz, all in 24-bit color.

In Table 4, video specific features are examined for the main Ethernet protocols.

Ethernet rules the data centric networking applications, with AFDX and TTE being the most natural choices for mission-critical systems. Currently, the rates of TTE and AFDX cannot accommodate common video resolutions, whereas BEE and TSN are defined for higher rates, but their lack of determinism (timing control) and certifiability eliminate them from consideration in this paper. When higher rates are available, ADFX or TTE would be suitable for some mission-critical video applications where only frame synchronous timing is required. This is typically the case when full frame buffers are used in the receiver, meaning they cannot be used for the most stringent timing classed that require line synchronous timing with nano-second accuracy on the line timing delivery.

## VIII. CONCLUSION

Each video and data bus has applications for which it is the most optimized technology. TTE and AFDX are the best avionics buses, but are not suitable for the most stringent class of mission-critical video.

System architects have the demanding job of deciding where to invest resources and must constantly ask the following questions. Should new technology be developed or adopted? Will old technology meet the system level requirements? Often, compromises are made due to budgets that forces a designer to mix both old and new technology. End-to-end latency must be a primary consideration given the increasing demands of video based real-time, avionics and mission systems. A latency budget for each device should be established, with consideration of where image buffering can be done and where it must be eliminated. Typically, strict line synchronous timing will be required when transmitting to a device where no frame buffering is possible due to latency or safety concerns, such as cockpit displays.

TABLE III. COMPARISON OF ETHERNET CAPABILITIES FOR CARRYING UNCOMPRESSED VIDEO

	Video Resolution		
	HD: 1920x1080 @ 60Hz	4K: 3840x2160 @ 60Hz	8K: 7680x4320 @ 25Hz
Bandwidth Required (no protocol)	3.73 Gbps	14.93 Gbps	24.88 Gbps
ARINC 818 Rate	4X (4.25 Gbps)	24X (21.0375 Gbps)	32X (28.05 Gbps)
TTE Rate	N/A	N/A	N/A
AFDX Rate	N/A	N/A	N/A
TSN Rate	10 Gbps	25 Gbps	40 Gbps



TABLE IV. VIDEO CENTRIC FEATURES AND SUITABILITY FOR AVIONICS

	Ethernet Protocols			
	<i>BEE</i>	<i>TTE</i>	<i>AFDX</i>	<i>TSN</i>
Frame Sync Timing	Possible	Yes, with jitter	Yes, with jitter	Yes, with jitter
Line Sync Timing	No	No	No	No
Pixel Sync Timing	No	No	No	No
Magnitude of Video Line Timing Jitter (in nano-seconds) at 1Gbps rate.	Unpredictable - depends on network size and complexity	~1,000 ns	~10,000 ns	Synchronous ~1,000 ns  Asynchronous ~10,000 ns
Pixel Type Supported	None natively	None natively	None natively	None natively
Video Centric Special Characters for video line and frame timing	None natively, must be defined in ICD	None natively, must be defined in ICD	None natively, must be defined in ICD	None natively, must be defined in ICD

Considering the available video and data bus options, ARINC 818 is the most flexible video-centric bus for low-latency, precisely timed mission-critical avionics and mission systems. It allows designers flexibility to convert to and from other buses when mixing old and new technology is required, and can help designers meet the most stringent latency demands of HDDs, HUDs, and HMDs. If low latency is a primary concern, then selecting a single video bus for the entire design reduces the protocol to protocol conversion latency.

ARINC 818 has been flying for 15 years in both commercial and military applications and has been certified to DAL A in dozens of applications. It is the official Avionics Digital Video Bus standard for commercial applications, and the defacto standard for military systems. It is now taking on the role as the video backbone of choice for complex, video-based, low-latency, and safety certifiable avionics and mission systems.

## IX. FUTURE WORK

The flexibility of ARINC 818 which makes it suitable as a video backbone for low-latency, mission-critical military and aerospace systems, also means that the implementation can be complicated because virtually any Interface Control Document (ICD) can be implemented, even custom, nonstandard video formats.

### A. Establish a Standardized Set of ICDs

Establishing a set (even if it is large) of standard ICDs required for high performance sensors, processors, and displays that are publicly available would help reduce the implementation complexity and reduce time and cost. ARINC 818 allows each project to define an ICD. This is typically a short document describing how the video resolution(s), pixel packing method, update rate, and timing. Airbus is currently spearheading an activity to design a standard set of ICD that designers can choose from and test tool manufacturers can certify that their tools support. This will be helpful across the industry.

### B. Standardize Sensor Interfaces

Reduce the number of resolutions, pixel packing modes, and link rates used. This is a subset of developing standard ICDs. Customized pixel packing can be accommodated by ARINC 818, however, this does not mean COTS test equipment can support it without modification. Having a standard set of ICDs, even if the list is long, provides both tool makers and system designers means to reduce risk and increase interoperability.

### C. MOSA and SOSA Adoption

The Modular Open System Approach (MOSA) and Sensor Open System Architecture (SOSA) lean heavily on the Ethernet protocols as the backbone their systems. As discussed above, Ethernet is an excellent choice, TTE in particular for mission-critical, low latency data applications, but it is not optimized for video and in many cases is not capable of implementing precise line synchronized video timing with nanosecond accuracy [1]. System integrators in the SOSA community are advocating for the formal adoption of ARINC 818 as a video bus.

## REFERENCES

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